AMENDMENTS TO THE CLAIMS

Please **CANCEL** claims 1-3 and 6-17 without prejudice or disclaimer.

The following is a complete list of all claims in this application.

1-3. (Cancelled)

4. (Previously Presented) A flat panel display, comprising:

a power unit generating a constant voltage;

a gate voltage generating unit generating a gate on/off voltage;

a controller comprising:

a signal processing unit receiving driving data and a driving control signal and generating RGB data, a scan control signal and a column control signal;

a gamma data generating unit generating digital gamma data with reference to the constant voltage from the power unit, the digital gamma data having a plurality of gradation values; and

a mixer unit mixing the digital gamma data and the RGB data to form a mixed signal, the digital gamma data arranged in a blanking section of the RGB data;

a scan driver unit receiving the scan control signal and the gate on/off voltage and generating a scan signal;

a column driver unit converting the digital gamma data into an analog gradation voltage and generating a column signal based on the column control signal, the RGB data and the analog gradation voltage; and

a flat display panel displaying an image based on the scan signal and the column signal.

5. (Previously Presented) The flat panel display of claim 4, wherein the column driver unit comprises a plurality of column driver ICs, and

each of the column driver ICs comprises:

a data diving unit receiving and dividing the mixed signal from the mixer unit into the RGB data and the digital gamma data;

a memory storing the digital gamma data from the data diving unit;

a decoder decoding the digital gamma data from the memory;

a first D/A converter converting the decoded digital gamma data into an analog gradation voltage;

a shift register sequentially shifting a timing pulse;

a data latch storing the RGB data from the data dividing unit and outputting the stored RGB data according to the timing pulse from the shift register;

a second D/A converter receiving the analog gradation voltage from the first D/A converter and the RGB data from the data latch, selecting the gradation value corresponding to the RGB data from the data latch and generating a gradation voltage based on the selected gradation value; and

a buffer buffering the gradation voltage from the D/A converter and generating the column signal.

6-17. (Cancelled)